CLAIMS:

1. A method of processing a semiconductor wafer comprising the steps of:

(a) providing a wafer having a planar top surface defined by a layer of a first material with elements of a second material embedded therein;

(b) etching at least a portion of said top surface with an etchant which preferentially attacks said first material so as form a new top surface with said elements of said second material protruding from surrounding portions of said new top surface; and

(c) optically locating one or more raised features on said wafer defined by said protruding second material elements or overlying said protruding second material elements.

2. The method as claimed in claim 1 further comprising the step of depositing one or more additional layers on said new top surface before said locating step.

3. The method as claimed in claim 2 wherein said step of optically locating said raised features includes directing light through one or more of said additional layers to said raised features and detecting light which has interacted with said raised features.

4. The method as claimed in claim 2 wherein said step of depositing one or more additional layers includes depositing an opaque lower additional layer of substantially uniform thickness so that said lower additional layer defines an upper surface having said raised features overlying the protruding second material elements.

5. The method as claimed in claim 4 wherein said step of depositing one or more additional layers includes the step of depositing one or more transparent layers over said upper surface of said opaque lower additional layer, and wherein said step of directing light includes directing light through

said one or more transparent layers to said raised features at said upper surface.

6. A method as claimed in claim 5 wherein said protruding second material elements project above the surrounding portions of said new top surface by a protrusion height of less than about 100 nm.

7. A method as claimed in claim 6 wherein said opaque lower additional layer has a thickness less than about ten times said protrusion height.

8. A method as claimed in claim 6 wherein said protrusion height is between about 20 nm and about 50 nm.

9. A method as claimed in claim 5 wherein said one or more transparent layers includes a layer of a photoresist.

10. A method as claimed in claim 4 wherein said lower additional layer is formed from a metallic material.

11. A method as claimed in claim 10 wherein said second material is metallic and said lower layer is deposited directly on said new top surface of said wafer, so that said metallic lower additional layer is contiguous with said elements formed from said second material.

12. A method as claimed in claim 11 wherein said second material and said metallic material of said lower layer consist essentially of copper.

13. A method as claimed in claim 2 wherein said one or more additional layers consist solely of transparent layers, wherein said raised features are defined by said protruding second material elements and wherein said locating step includes directing light through said transparent layers to said protruding second material elements.

14. A method as claimed in claim 13 wherein said step of depositing one or more additional layers include depositing a transparent dielectric layer and then depositing a layer of a photoresist.

15. A method as claimed in claim 14 wherein said step of depositing one or more additional layers further includes depositing an antireflection coating on said transparent dielectric layer before depositing said photoresist.

16. A method as claimed in claim 14 wherein said transparent dielectric layer includes an oxide.

17. A method as claimed in claim 1 wherein said wafer includes at least one functional region and at least one alignment region, said elements formed from said second material include one or more alignment marks disposed in said at least one alignment region, and said step of etching said top surface is performed only in said at least one alignment region.

18. A method as claimed in claim 1 wherein said step of etching said top surface is performed over the entire top surface.

19 A method as claimed in claim 1 wherein said raised features form a diffraction grating and said step of detecting light includes detecting light diffracted by said grating.

20. A method as claimed in claim 2 wherein said locating step is performed so as to locate the wafer in the frame of reference of a processing apparatus, the method further comprising forming additional features on the wafer at least in part by operation of said processing apparatus.

21. A method as claimed in claim 20 wherein said processing apparatus is a wafer stepper and said step of forming additional features includes applying patterned illumination to the wafer.

22. A method of processing a semiconductor wafer comprising the steps of:

(a) providing a starting wafer including a top layer of dielectric with metallic damascene elements therein, said layer having a planar top surface, said dielectric and said damascene elements being exposed at said top surface;

(b) etching said top surface with an etchant which preferentially attacks said dielectric so as to form a new top surface with said damascene elements protruding from said dielectric; and

(c) depositing a metallic layer of substantially uniform thickness on said top surface so that said metallic layer defines an upper surface having raised features overlying said damascene elements projecting.

23. A method as claimed in claim 22 further comprising the steps of locating said raised features and registering the wafer with processing apparatus based on the detected locations.

24. A method as claimed in claim 22 further comprising the step of depositing a photoresist layer over said metallic layer before said locating step, said step of locating including directing light through said photoresist layer.

25. A method as claimed in claim 22 wherein said step of providing a starting wafer includes chemical mechanical polishing.

26. A method as claimed in claim 22 wherein said step of etching said top surface includes exposing said damascene features and said dielectric at said top surface to an etchant non-selectively, over the entire top surface of the wafer.

27. A method as claimed in claim 22 wherein said starting wafer includes at least one functional region and at least one alignment region, said damascene elements include alignment marks disposed in said at least one alignment region and functional damascene elements in said at least one functional region, said step of etching said top surface is performed in said at least one alignment region but not in said at least one functional region.

28. A method as claimed in claim 22 wherein said dielectric includes SiO_2 at said top surface.

29. A method as claimed in claim 28 wherein said damascene features include copper.

30. A method as claimed in claim 29 wherein said etching step includes exposing said top surface to an etchant selected from the group consisting of hydrofluoric acid solutions and fluorine-containing plasmas.

31. A method as claimed in claim 22 wherein said step of etching said top surface is performed so as to leave said damascene features protruding above said dielectric by 20 to 50 nm.

32. A method as claimed in claim 31 further comprising the step of depositing a photoresist layer between 100 nm and 1 μm thick over said metallic layer before said locating step, said step of locating including directing light through said photoresist layer

33. A method as claimed in claim 32 wherein said metallic layer is less than about 500 nm thick.

34. A method of processing a semiconductor wafer comprising the steps of:

(a) providing a starting wafer including a top layer of dielectric with polysilicon elements therein, said layer having a planar top surface, said dielectric and said polysilicon elements being exposed at said top surface;

(b) etching said top surface with an etchant which preferentially attacks said dielectric so as to leave said top surface with said polysilicon elements protruding from said dielectric; and

(c) depositing a transparent oxide layer on said top surface so that said polysilicon elements project into said oxide layer; and then

(d) locating said polysilicon elements by directing light through said oxide layer and detecting light which has interacted with said polysilicon elements, and registering the

wafer with processing equipment based at least in part upon the locations of the polysilicon elements.

35. A method as claimed in claim 34 further comprising the step of depositing a photoresist over said transparent oxide layer before said locating step.

36. A method as claimed in claim 34 wherein said polysilicon elements protrude above said nitride dielectric layer by a protrusion height less than about 100 nm.